xxxFN (JEDEC SOP) is not available in

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74LVX32F,TC74LVX32FN,TC74LVX32FT

Note:

Quad 2-Input OR Gate

The TC74LVX32F/ FN/ FT is a high-speed CMOS 2-input OR gate fabricated with silicon gate CMOS technology. Designed for use in 3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

This device is suitable for low-voltage and battery operated systems.

The internal circuit is composed of 4 stages including buffer output, which provide high noise immunity and stable output.

An input protection circuit ensures that 0 to 5.5V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High-speed: $t_{pd} = 4.4 \text{ ns (typ.) (V}_{CC} = 3.3 \text{ V})$
- Low power dissipation: $I_{CC} = 2 \mu A \text{ (max) (Ta} = 25 ^{\circ}\text{C)}$
- Input voltage level: V_{IL} = 0.8 V (max) (V_{CC} = 3 V)

 $V_{IH} = 2.0 \text{ V (min)} (V_{CC} = 3 \text{ V})$

- · Power-down protection provided on all inputs
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Low noise: VOLP = 0.5 V (max)
- ullet Pin and function compatible with 74HC32

SOP14-P-300-1.27A

SOP14-P-300-1.27

TC74LVX32FN

SOL14-P-150-1.27



TC74LVX32FT

 SOP14-P-300-1.27A
 : 0.18 g (typ.)

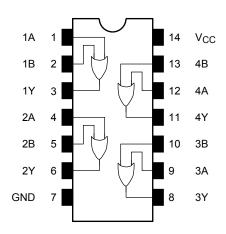
 SOP14-P-300-1.27
 : 0.18 g (typ.)

 SOL14-P-150-1.27
 : 0.12 g (typ.)

 TSSOP14-P-0044-0.65A
 : 0.06 g (typ.)

TSSOP14-P-0044-0.65A

Pin Assignment (top view)



IEC Logic Symbol

1A	(1)	≥ 1	(3)
1B	(2)		1Y
2A	<u>(4)</u> (5)		(6) 2Y
2B	(9)		21
3A	(10)	•	(8) 3Y
3B	(12)		
4A	(13)		(11) 4Y
4B			

Truth Table

Inp	Outputs				
Α	В	Υ			
L	L	L			
L	Н	Н			
Н	L	Н			
Н	Н	Н			

Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit	
Supply voltage range	V_{CC}	-0.5 to 7.0	V	
DC input voltage	V _{IN}	-0.5 to 7.0	٧	
DC output voltage	V _{OUT}	-0.5 to $V_{CC} + 0.5$	٧	
Input diode current	I _{IK}	-20	mA	
Output diode current	I _{OK}	±20	mA	
DC output current	lout	±25	mA	
DC V _{CC} /ground current	I _{CC}	±50	mA	
Power dissipation	P_{D}	180	mW	
Storage temperature	T _{stg}	-65 to 150	°C	

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.



Recommended Operating Conditions (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V _{CC}	2.0 to 3.6	V
Input voltage	V _{IN}	0 to 5.5	V
Output voltage	V _{OUT}	0 to V _{CC}	V
Operating temperature	T _{opr}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 100	ns/V

Note: The recommended operating conditions are required to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics

Characteristics		Symbol	Test Condition			Ta = 25°C			Ta = -40 to 85°C		Unit	
				V _{CC} (V)	Min	Тур.	Max	Min	Max			
					2.0	1.5	_	_	1.5	_		
	H-level	V _{IH}		_	3.0	2.0	_	_	2.0	_		
Input voltage					3.6	2.4	_	_	2.4	_	V	
imput voltage	L-level				2.0	_	_	0.5	_	0.5	V	
		V _{IL}		_	3.0	_	_	0.8	_	0.8		
					3.6	_	_	0.8	_	0.8		
	H-level			$I_{OH} = -50 \mu A$	2.0	1.9	2.0	_	1.9	_		
		VoH	V _{IN} = V _{IH} or V _{IL}	V _{IN} = V _{IH} or V _{II}	I _{OH} = -50 μA	3.0	2.9	3.0	_	2.9	_	
Output voltage				I _{OH} = -4 mA	3.0	2.58	_	_	2.48	_	V	
Output voltage		V _{OL}	$V_{IN} = V_{IL}$	$I_{OL} = 50 \mu A$	2.0	_	0	0.1	_	0.1	V	
	L-level			I _{OL} = 50 μA	3.0	_	0	0.1	_	0.1		
				I _{OL} = 4 mA	3.0	_	_	0.36	_	0.44		
Input leakage current		I _{IN}	V _{IN} = 5.5 V or GND		3.6		_	±0.1		±1.0	μА	
Quiescent supply current		Icc	$V_{IN} = V_{CC}$	or GND	3.6	_	_	2.0	_	20.0	μΑ	

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AC Characteristics (input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol Test Condition				Ta = 25°C			Ta = -40 to 85°C		Unit
			V _{CC} (V)	C _L (pF)	Min	Тур.	Max	Min	Max	
	t _{рLН}		2.7	15	_	5.8	10.7	1.0	13.5	- ns
Propagation delay time				50	_	8.3	14.2	1.0	17.0	
Fropagation delay time	4		3.3 ± 0.3	15	_	4.4	6.6	1.0	8.0	
	^t pHL			50	_	6.9	10.1	1.0	11.5	
Output to output skew	t _{osLH}	t _{osLH} (Note 1)	2.7	50	_	_	1.5	_	1.5	ns
Output to output skew	t _{osHL}	(Note 1)	3.3 ± 0.3	50	_	_	1.5	_	1.5	115
Input capacitance C _{IN}				(Note 2)	_	4	10	_	10	pF
Power dissipation capacitance C _{PD}			(Note 3)	_	14	_	_	_	pF	

Note 1: Parameter guaranteed by design.

 $(t_{\text{OSLH}} = |t_{\text{pLHm}} - t_{\text{pLHn}}|, \ t_{\text{OSHL}} = |t_{\text{pHLm}} - t_{\text{pHLn}}|)$

Note 2: Parameter guaranteed by design.

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

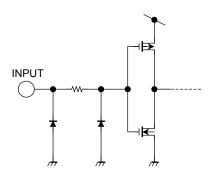
Average operating current can be obtained by the equation:

 $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per gate)}$

Noise Characteristics (Ta = 25°C, input: $t_r = t_f = 3$ ns, $C_L = 50$ pF)

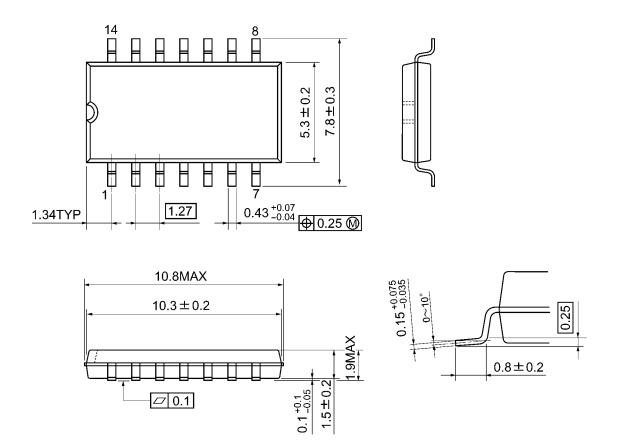
Characteristics	Symbol	Test Condition	V _{CC} (V)	Тур.	Limit	Unit
Quiet output maximum dynamic V_{OL}	V _{OLP}	_	3.3	0.3	0.5	V
Quiet output minimum dynamic V_{OL}	V _{OLV}	_	3.3	-0.3	-0.5	٧
Minimum high level dynamic input voltage $V_{\mbox{\scriptsize IH}}$	V_{IHD}	_	3.3	_	2.0	٧
Maximum low level dynamic input voltage V_{IL}	V_{ILD}	_	3.3		0.8	٧

Input Equivalent Circuit



Package Dimensions

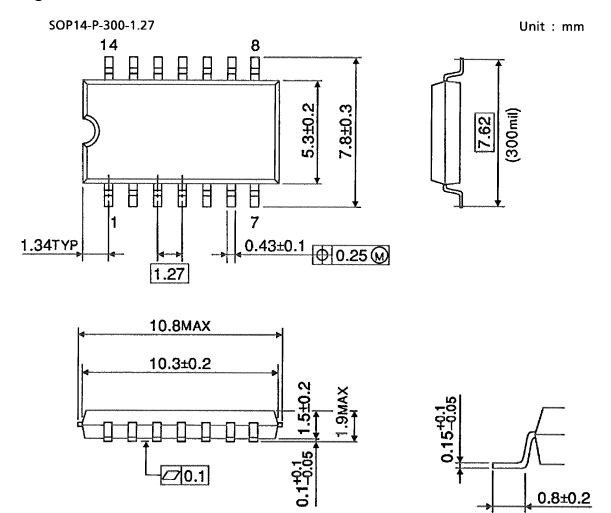
SOP14-P-300-1.27A Unit: mm



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Weight: 0.18 g (typ.)

Package Dimensions

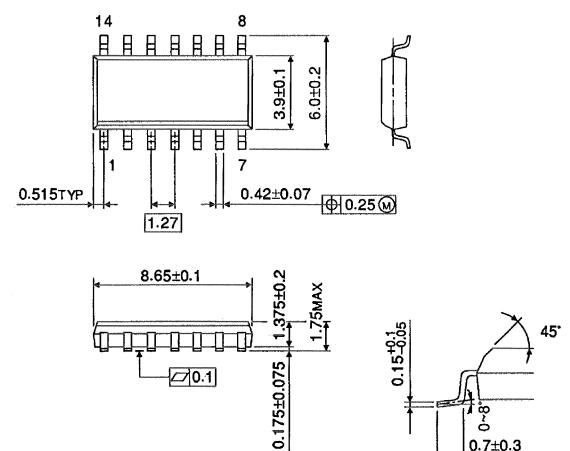


Weight: 0.18 g (typ.)

7 ‰ ∂ 0.7±0.3

Package Dimensions (Note)

SOL14-P-150-1.27 Unit: mm



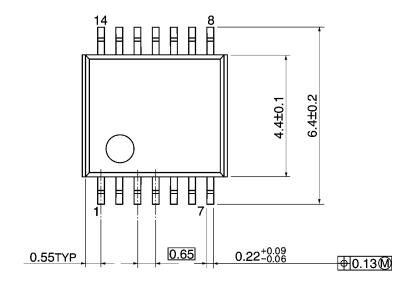
This package is not available in Japan. Note:

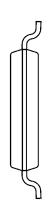
Weight: 0.12 g (typ.)

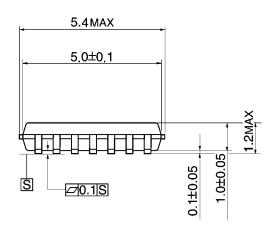
Package Dimensions

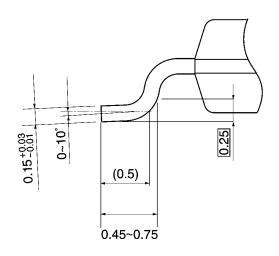
TSSOP14-P-0044-0.65A

Unit: mm









Weight: 0.06 g (typ.)

Note: Lead (Pb)-Free Packages

SOP14-P-300-1.27A SOL14-P-150-1.27 TSSOP14-P-0044-0.65A

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20070701-EN

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